



Press Release

RAPID BRIDGE INTRODUCES LIQUIDCELL LIBRARY TO BRING UNPARALLELED FLEXIBILITY TO CHIP DESIGN AT 40 NANOMETER PROCESS NODE

Metal-Programmable LiquidCell Library Offers Superior Performance and Speed to Market

SAN DIEGO, August 26, 2009 --- Rapid Bridge, an innovator in advanced semiconductor design and development processes, announced today that its revolutionary LiquidCell™ library is now available at 40nm process node. LiquidCell offers chip designers optimal performance, power, area, yield and unparalleled flexibility to reduce cycle time. LiquidCell consists of a metal-programmable sea of transistors that can be configured into millions of usable elements from a library of over 700 standard cells.

Metal-Programmability Saves Time and Money

The LiquidCell library offers superior performance with the added feature of metal configurability to dramatically enhance speed to market. Utilizing the sea of transistors, LiquidCell allows designers to make full logic changes using metal masks only – reducing the cycle time and costs associated with chip spins and derivative products. For example, LiquidCell allows chip designers to tapeout and validate ICs before a Standard is finalized and then, once the Standard is finalized, release a fully compliant product ahead of the competition with only a few metal layer spins. With LiquidCell, Rapid Bridge customers can beat their competition to market with a fully verified system solution.

“We have designed LiquidCell to be high performing and as flexible as possible,” said Ramin Absari, chief operating officer of Rapid Bridge. “Designers can both enjoy the ‘Customer-Owned Tooling (COT)-like’ performance and have the freedom to make blocks exactly the size required – eliminating extra pipes, power and other inefficiencies associated with macrocell design.”

System on a Chip Approach

The LiquidCell library can be used for any ASIC design and has been optimized to work within a System on Chip (SoC) environment. LiquidCell addresses the challenges associated with high-speed designs. The LiquidCell core is fast enough to synthesize register maps or any demanding block that requires high-performance libraries. The entire

LiquidCell library of over 700 cells, enabling more than 160 functions, is designed to work together, is fully ATPG/DFT-compliant, supports clock tree insertion, and is compatible with industry standard EDA tools and flows.

Low Risk, High Support

Rapid Bridge's LiquidCell library includes the most commonly used elements in standard synthesis libraries. Translation tables ensure competitive performance and a seamless transition to any internal flow. Rapid Bridge provides customers with full modeling support to deliver a high-yield, low-cost solution.

"Rapid Bridge's LiquidCell platform provides much higher performance than commonly used programmable gate arrays," continued Absari. "The exact same blocks can be used on LiquidASIC™, LiquidSoC™ or in a COT environment eliminating the risk in going from sample solution to production."

Availability

The LiquidCell library is offered in both high performance and low power versions. LiquidCell is available at TSMC for 90nm, 65nm, and 40nm nodes. For more information, contact sale-support@rapidbridge.com.

About Rapid Bridge

Rapid Bridge is a semiconductor technology company with a unique approach to addressing the industry's issues of cost, performance, power and time to market. Rapid Bridge's patented technology is baked into the product portfolio: LiquidIP™, LiquidASIC™ and LiquidSoC™. LiquidIP is a robust IP portfolio which includes the smallest and highest performing IPs in the industry. LiquidASIC lowers cost barriers and includes a complete collection of pre-defined ASIC platforms, interface subsystems and foundations IPs. LiquidSoC provides the industry's most cost efficient SoCs with customer-defined die size and IP resources, regular layout structures, and full programmability. Rapid Bridge enables the industry's genius. For more information on Rapid Bridge, visit us at www.rapidbridge.com.

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