

## CEI-6 / XAUI Subsystems

v1.3

### Features / Benefits

- IEEE802.3ae Compliant
- 1.06-6.4 Gbps for CEI-6/XAUI applications
- Full, Half and Quarter Rate options
- Very low jitter generation
- Adaptive Receiver equalization for enhanced jitter tolerance
- Amplitude and pre/post-emphasis options
- Eye width mapping and on chip jitter test features
- Power saving modes
- Signal detection
- ±100 ppm offset
- 8-, 10-, 16-, 20-bit parallel interface
- 8B10B Encode/Decode, Comma Detection and symbol alignment
- BIST circuitry with multiple pattern generation capabilities
- Multiple loopback test circuitries
- Multiple error status signals
- IEEE1194.1 and 1194.6 DC and AC JTAG support

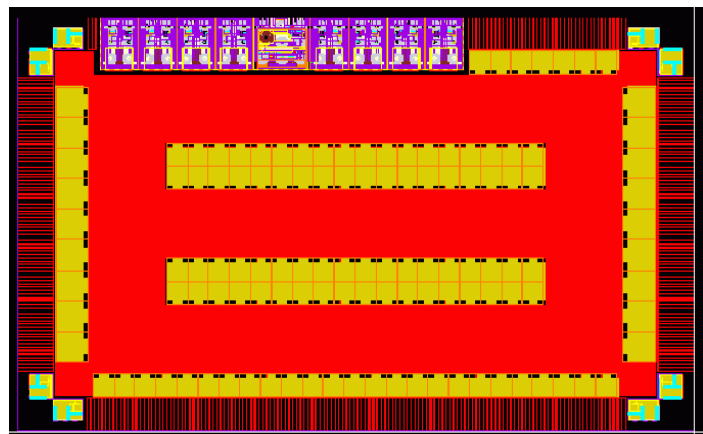
### Applications

- 10GbE applications
- Backplane applications
- XENPAK

### Product Description

The Rapid Bridge 10 Gigabit (X) Attachment Unit Interface (XAUI) is compliant with the IEEE802.3ae 10GbE specification. XAUI is the standard for connecting to an Ethernet MAC on a printed circuit board. This PHY consists of a hardened Physical Media Attach (PMA) layer that is programmed to meet different system link budgets and configuration requirements, and a soft Physical Coding Sublayer (PCS) that is intended to be programmed for different applications and form factors. Multiple 4-lane configurations are available in LiquidASIC offering. These may be further extended or modified to meet specific requirements in LiquidSoC offering. A wide range of transmit amplitudes and pre- and post- emphasis (de-emphasis), coupled with receiver equalization options, allow for optimum link budgeting of the overall system. PIPE interface is programmable to 8 or 16 bits. The Clock and Data Recovery (CDR) circuit allows for different levels of filtering and loop bandwidths to accommodate ppm offset. This PHY also supports Spread Spectrum Clock source. The 8B/10B encoder and decoders are provided as part of the PCS layer to allow for full programmability and function extension. A wide range of reference clock inputs are supported to meet different system requirements and clocking schemes. PCS layer also incorporates comma detection and word symbol alignment. The XAUI PHY incorporates high-level built-in test functions. It supports three different loopback modes: serial loopback, line-side loopback and parallel loopback. A centralized BIST consists of a pattern generator on the transmit side and a pattern verifier block on the receive side. Multiple patterns in support of different standards may be generated by the BIST block. The pattern verifier block aligns itself with the generated pattern and records number of mismatches in the captured data. This PHY also supports IDDQ testing and DC and AC JTAG in accordance to IEEE1149.1 and 1149.6. All receive and transmit on-die terminations are automatically calibrated to ensure proper return loss across the frequency spectrum. Architecture of XAUI results in low level of jitter generation that is well below the IEEE802.3ae requirements for both deterministic and sinusoidal jitter components.

XAUI Macro in a LiquidSoC™





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### Complete Subsystem Solution

Rapid Bridge 10 Gigabit Attachment Unit Interface serial link PHY is part of LiquidSerDes family and is offered as an integrated part of LiquidASIC and LiquidSoC platforms. This PHY provides a wide range of programmability that allows users to meet different system requirements. LiquidSerDes is register- and metal-programmable and benefits from wide range of amplitude, pre- and post- emphasis and receiver equalization settings that allows for link optimization beyond a specific standard. This PHY may be operated at full, half or quarter rate, resulting in internal power optimization and a wide range of reference clock selections. The parallel interface may be operated at 8, 10, 16 or 20 bits for different core signaling frequencies. This design also incorporates additional power saving features such as electrical idle detection at different signaling levels and beacon signaling. LiquidSerDes incorporates a comprehensive set of Built In Self Test (BIST) functions with multiple pattern and noise generation capabilities that simplifies system validation. Internal BIST is complemented with different loopback capabilities, providing comprehensive fault coverage. Core boundaries utilize scan registers, and DC and AC JTAG are supported to allow for board-level continuity testing. XAUI PHY is complemented with third party MAC layer to meet end user's specific system needs.

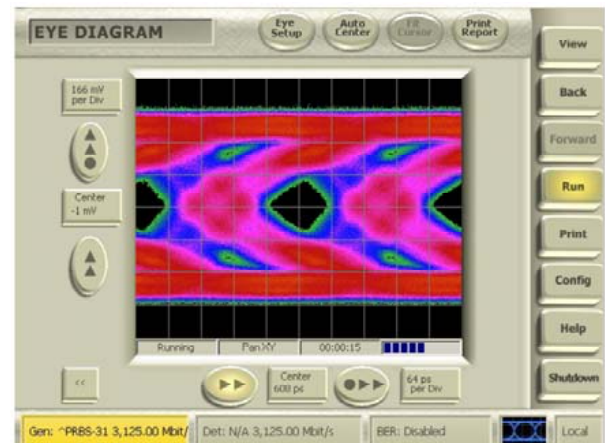
### For More Information. . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

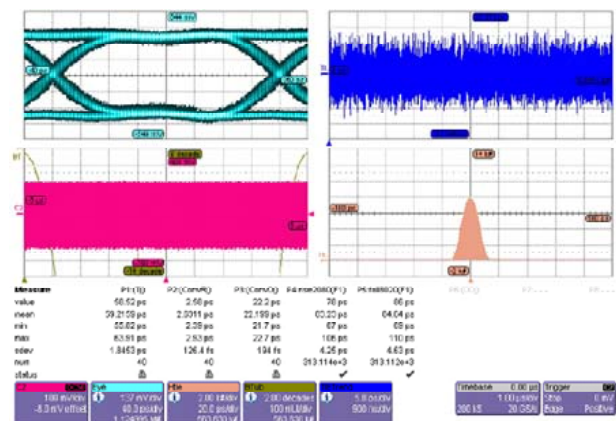
sales-support@rapidbridge.com or visit www.rapidbridge.com

### Performance Beyond the Past

Rapid Bridge XAUI serial link is a tightly integrated subsystem that addresses the interaction between different analog, mixed-signal and digital blocks. Operating ranges may be seamlessly extended in support of double-XAUI applications. Different silicon characterizations over PVT have been performed to eliminate any potential design weaknesses. LiquidSerDes meets ESD of 2kV HBM and 500 CDM as part of LiquidASIC and LiquidSoC platforms.



### Stressed Receiver Jitter Tolerance



### XAUI Jitter Generation Bathtub