

PCI_Express Gen/II Subsystems

v1.3

Features / Benefits

- 2.5Gbps/5.0Gbps
- PCI Express v1.1/v2.0 compliant
- Amplitude and de-emphasis control
- Electrical Idle signaling and detection
- Receiver detection circuitry
- P0, P0S, P1, and P2 Power saving/modes
- Supports Mobile Graphics Low-Power addendum
- Supports Wireless Form Factor extension
- Spread Spectrum Clocking
- ± 600 ppm clocking offset
- Port Bifurcation factors of 1X, 4X, or 8X
- PIPE Compliant interface
- 8B/10B encode/decode, comma detection and symbol alignment
- PCI_Express compliant BIST circuitry patterns
- Multiple loopback test circuitries
- Multiple error status signals
- IEEE1194.1 and 1194.6 DC and AC JTAG support

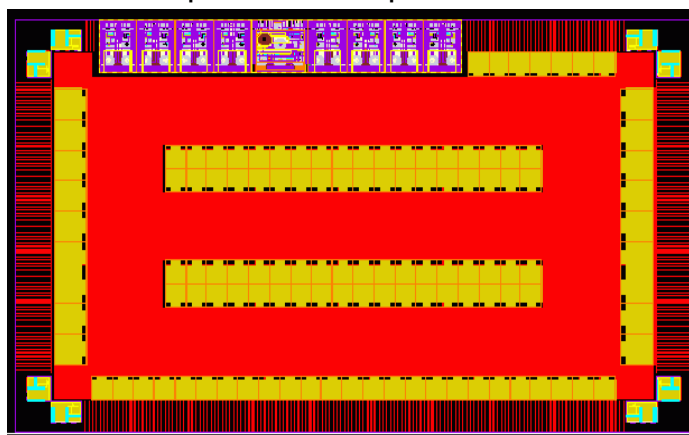
Applications

- PCI Express v1.1 Root Complex or End Point Applications
- Desktop, mobile and wireless applications

Product Description

Rapid Bridge 2.5/5.0Gbps PCI Express v1.1/v2.0 serial link PHY is suitable for Root Complex and End Point applications. This PHY provides support for a number of PCI Express addendums and extensions including Mobile Graphics Low power and Wireless Form factor applications. This PHY is comprised of a hardened Physical Media Attach (PMA) layer that is programmed to meet different system link budgets and configuration requirements, and a soft Physical Coding Sublayer (PCS) that is intended to be programmed for different applications and form factors. Different lane configurations from 1 to 32 lanes are available in LiquidASIC offering. These may be further extended or modified to meet specific requirements in LiquidSoC offering. A wide range of transmit amplitude, pre- and post- emphasis (de-emphasis), coupled with receiver equalization options, allows for optimum link budgeting of the overall system. The PIPE interface is programmable to 8 or 16-bits. Clock and Data Recovery (CDR) circuit allows for different levels of filtering and loop bandwidths to accommodate ppm offset. This PHY also supports Spread Spectrum Clock sources. 8B/10B encoder and decoders are provided as part of the PCS layer to allow for full programmability and function extension. A wide range of reference clock inputs are supported to meet different system requirements and clocking schemes. The PCS layer also incorporates comma detection and word symbol alignment. Electrical idle detection and beacon signaling are supported by receivers and transmitters, allowing for PCI Express power saving modes (P0, P0S, P1 and P2). For Root Complex applications, port bifurcation is supported where multiple lanes are configured into individual links of 1 or more lanes each. PCI Express incorporates high-level built-in test functions. It supports three different loop back modes: serial loopback, line-side loopback and parallel loop back. A centralized BIST consists of a pattern generator on the transmit side and a pattern verifier block on the receive side. Multiple patterns in support of different standards may be generated by the BIST block. The pattern verifier block aligns itself with the generated pattern and records the number of mismatches in the captured data. This PHY also supports IDDQ testing and DC and AC JTAG in accordance to IEEE1149.1 and 1149.6.

PCI Express Macro in a LiquidSoC



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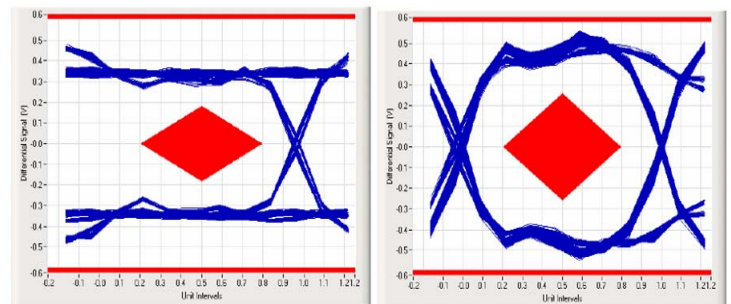
Complete Subsystem Solution

The Rapid Bridge 2.5/5.0Gbps PCI Express v1.1/v2.0 Serial Link PHY is part of the LiquidSerDes family and is offered as an integrated part of the LiquidASIC and LiquidSoC platforms. This LiquidSerDes PHY provides a wide range of programmability that allows users to meet different system requirements.

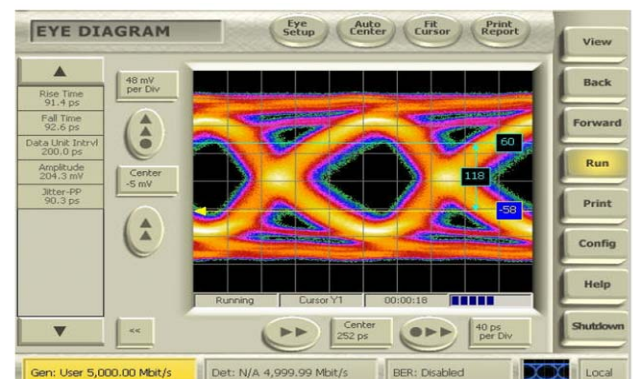
LiquidSerDes is register- and metal-programmable and benefits from wide range of amplitude, pre- and post- emphasis and receiver equalization settings that allow for link optimization beyond a specific standard. This PHY may be operated at full, half or quarter rate, resulting in internal power optimization and wide range of reference clock selections. The parallel interface may be operated at 8, 10, 16 or 20 bits for different core signaling frequencies. This design also incorporates additional power saving features such as electrical idle detection at different signaling levels and beacon signaling. LiquidSerDes incorporates a comprehensive set of Built In Self Test functions with multiple pattern and noise generation capabilities, which simplifies system validation. Internal BIST is complemented with different loopback capabilities, providing comprehensive fault coverage. Core boundaries utilize scan registers and DC and AC JTAG are supported to allow for board-level continuity testing. PCI Express PHY is complemented with third-party transaction and link layers to meet user's specific system needs.

Performance Beyond the Past

PCI Express Gen/II PHY is a tightly integrated subsystem that addresses the interaction between different analog, mixed-signal and digital blocks. This approach yields a homogenous subsystem that provides optimum performance, power and area. Metal-programmability further allows architectural flexibility and feature enhancements that otherwise would not be possible. Different silicon characterizations over PVT has been performed to eliminate any potential design weaknesses. LiquidSerDes meets the ESD specifications of 2kV HBM and 500 CDM as part of LiquidASIC and LiquidSoC platforms.



PCI Express GENI worst case non-transitional and transitional eye-diagrams



PCI Express GENII Receiver Jitter Tolerance

For More Information. . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

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