LiquidPHY USB 2.0

V1.1

Physical Layer Features

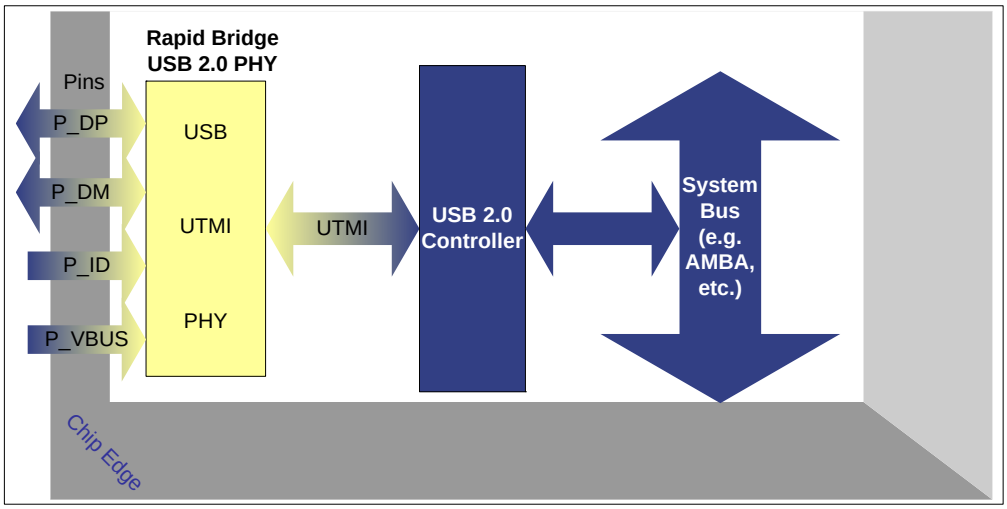
- Fully compliant with USB 2.0 (latest revision) specifications
- On-The-Go (OTG) Host, embedded Host, or Device applications
- Supports HS (480MbpS), FS (12MbpS), and LS (1.5MbpS) HOST and DEVICE applications
- Includes all power and ground pads
- 60mW peak power (HS TX)
- 15kV ESD board level
- Fast-tracking CDR (over 10k ppm)
- Configurable BIST (HS, FS, & LS); times as low as 300µS including CDR sensitivity
- Shortened suspend wake up
- Core-side interface complies with UTMI+ (USB2.0 Transceiver Macrocell Interface Plus) level3 specifications
  - Elastic Buffer
  - Reset Detection
  - Integrated selectable termination resistors
  - Sync detector
  - NRZ encoder/decoder
  - Serializer/deserializer
  - Control state machine

Product Description

The Rapid Bridge USB 2.0 LiquidPHY is a multispeed transceiver that combines seamlessly with our patented, highly customizable IO architecture: it is programmed into 12 interface templates within the Rapid Bridge programmable IO ring. Unlike traditional PHYs, our integrated solutions give our customers complete freedom to tailor their designs (much like any Standard Cell approach). The PHY's area- and power- efficient design is tightly controlled over process corners and benefits from full metal programmability.

The result is a significantly reduced design and verification effort. The Rapid Bridge approach yields a correct-by-construction solution, and addresses local transistor variation that is common in sub-micron technologies.
This results in the industry's smallest footprint: **<0.2mm^2**

Block Diagram



The Rapid Bridge USB 2.0 PHY solution is a comprehensive interface intended for host, embedded host, and device applications; it integrates calibrated pull-up and pull-down resistors and power-down mode for battery-operated applications.

Deliverables

- Datasheet
- Application notes
- Interface Liberty
- Verilog
- LEF
- GDSII
- CDL

Applications

- Keyboards
- Mice
- PDAs
- Game consoles and joysticks
- Scanners
- Digital cameras
- Printers
- Personal media players
- Flash drives
- External hard drives

Note: *a charge pump and generation of the 5V to support external USB devices must be handled externally. The USB pins have enhanced on-die ESD protection that can be further complemented with onboard protection in order to achieve the necessary ±15 kV.*

Product Brief

LiquidPHY™ USB2.0

Functionality

This subsystem is comprised of receive and transmit paths. The transmit path consists of front end blocks and output drivers.

The front-end block performs the logical operations for registering the parallel data, shifting and holding the data, bit stuffing, and encoding the data (using NRZI format). The encoded, serialized data stream is transmitted by the output driver in an LS, FS or HS data rate (differentially or single-ended) according to the application.

The receive path consists of the input receiver that receives the data (differentially or single- ended) according to the application. An integrated multi-phase PLL and CDR circuit are used to recover the clock and data.

The recovered HS or FS/LS bit streams feed the back-end block (which consists of a multiplexer and elastic buffer to accommodate the HS and FS/LS applications, NRZI decoder logic, bit un-stuffer, shift and hold register). A squelch function is also built into the receiver path.

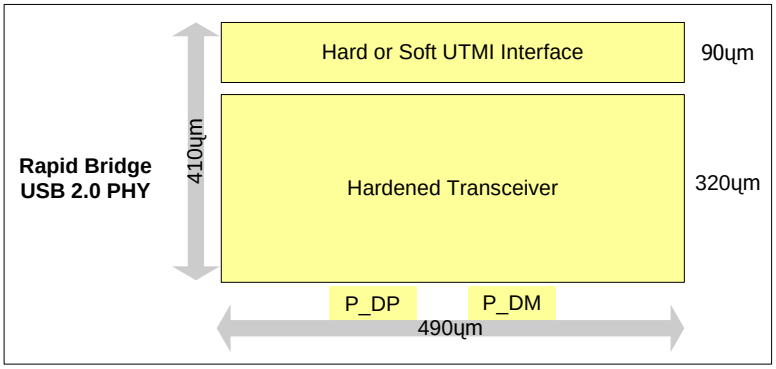
Transmit and receive paths have dedicated state machines that control the operation of the respective paths. Common control logic is used to control the behavior of the PHY (e.g. power management, termination control, bit stuffing/un-stuffing, and encoding/ decoding to NRZI format).

Feature Benefits

Feature	Benefit
Patent-pending drivers	Improved signal quality
Constant output impedance during transitions	Improved transmission line matching
Digitally regulated slew rate control:	FS slew = 13nS
	LS slew = 110nS

Pre-Configured and Programmable Regions

As shown below, the Rapid Bridge USB 2.0 solution includes both pre-configured and programmable areas, all within the industry's smallest footprint. Typically, this PHY is paired with a (crb) PLL and a crystal oscillator.



Testing

The PHY is UTMI+level3-interface-compatible and can be validated with other link layers. The test chip will accommodate on-chip and off-chip controllers to ease certification and address link layer selection.

USB2.0 PHY production test:

- Vendor test pints
- Scan and ATPG
- Analog test bus
- One-time impedance trimming
- One-time envelope detector trimming with internal calibration option
- One-time HS TX-level trimming
- High coverage BIST for HS, FS, and LS modes (including CDR sensitivity testing)

For More Information. . .

Regarding the Liquid family of products, please contact Rapid Bridge at: sales-support@rapidbridge.com or visit www.rapidbridge.com