

LiquidPHY DDRIII Subsystem

V1.5

Features

Physical Layer

- 1600 Mbps
- Pre-configured bus in 32/64/72 bit widths
- 128Mb-4Gb addressable locations, single or dual ranks
- Impedance-calibrated 120Ω, 20/30/40/60Ω ODT
- Calibrated output impedance of 40/34Ω
- ¾ latency on during write cycle
- Minimal read latency achieved via parameterized pipelining
- High clock rates with minimal routing constraints
- Optional pipe insertion at the controller interface for ease of timing
- Integrated master and slave DLL with supply regulation and resolution up to 10 ps.
- Programmable delayed address and command lines
- Fully programmable within Rapid Bridge LiquidASIC and LiquidSoC
- JESDEC79-3A compatible
- Fully DFI-compliant

Controller (NWL)

- Maximizes bus efficiency via Look-Ahead command processing, Bank Management, Auto-Precharge and Additive Latency support
- Full run-time configurable timing parameters and memory settings
- Supports ODT and 2T timing
- Low gate count
- Source code available
- Customization services available

Product Description

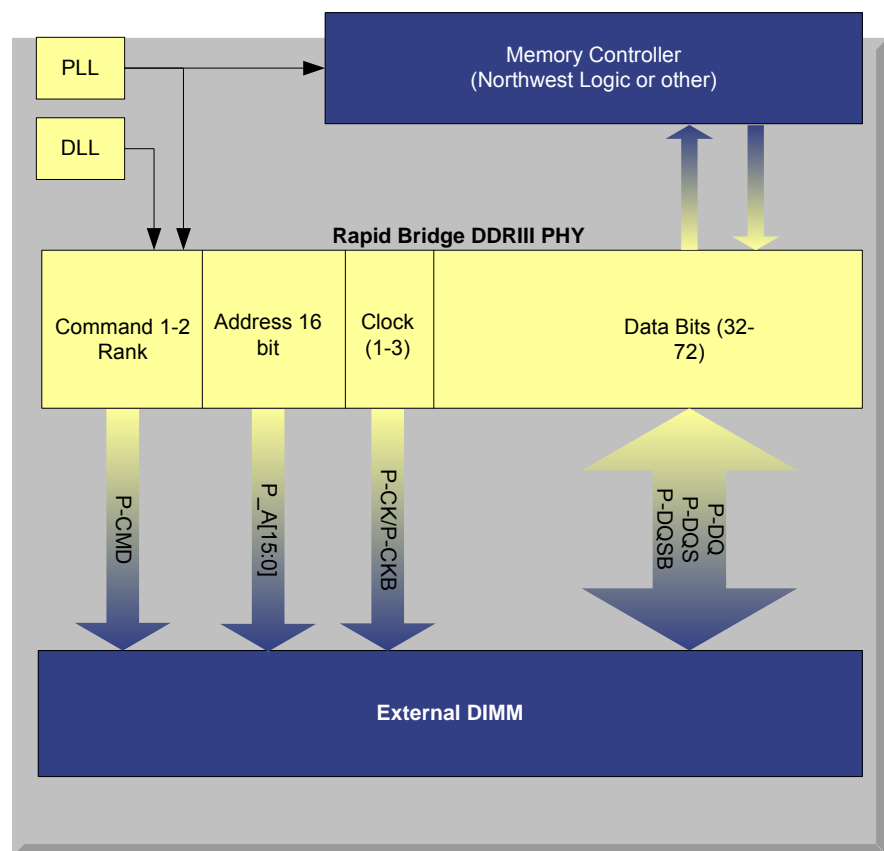
Double Data Rate 3 (DDRIII) is a high-bandwidth data transfer specification governed by JEDEC79-3C; it connects a Dynamic Random Access Memory (DRAM) chip or Dual Inline Memory Module (DIMM) to a processing chip in an electronic device or system.

The Rapid Bridge DDRIII LiquidPHY subsystem combines our patented IO architecture with PHY functions, test circuitry, and a third-party memory controller. This combination can be programmed and tested (via BIST) for a variety of applications. The physical implementation may be customized to meet different chip architectures and may wrap around single or multiple corners.

The result is significantly reduced design and verification of memory subsystems. The Rapid Bridge approach yields a correct-by-construction solution that can be configured by the end user to a specific application for maximum silicon efficiency.

The Rapid Bridge DDRIII is fully DDR PHY Interface (DFI) compliant.

DDRIII Within an SoC



Memory Controller

The Rapid Bridge DDRIII PHY is interoperable with third-party controllers including Northwest Logic's and Denali's DDRIII controllers.

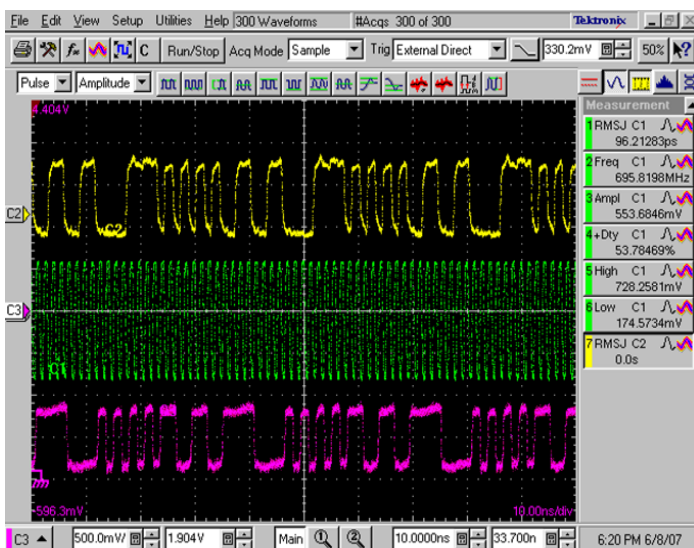
Benefits

The Rapid Bridge DDRIII PHY simplifies the communication to DIMMs and SDRAMs:

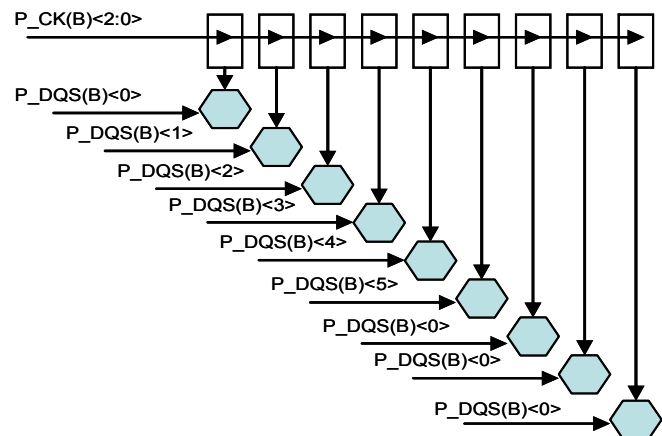
Feature	Benefit
Best-in-class write and read latencies: ¼ cycle write latency, programmable 4 deep ring FIFO at the read interface.	Allows for optimum boundary alignment and link budgeting over a wide range of implementations
On Die Termination (ODT) and impedance-calibrated output drivers.	Ensures optimum termination and signal integrity.
Optional core side pipeline stage.	Simplifies the controller and PHY interface.
Regulated master and slave Delay Lock Loops with metal-programmable range and resolution.	Simplifies the top-level link budgeting of the interface, maintains optimum resolution across PVT (independent of potential noise on the ASIC's core supply).
Integrated multi-phase PLL.	Allows for a ½ clocking rate that improves the overall power consumption of the logic section.
Optional ½ strength drive and matched calibrated pull-up and pull down-drivers.	Potentially reduces power consumption.
Address and command lines may be pipelined and delay controlled.	Optimizes the timing of the interface and load requirements.
Per byte programmable read loops.	Minimizes the impact of any input and output delay across PVT and board delays associated with CLK and DQS lines.
Per byte high resolution, 10ps per stage, PVT controlled write leveling DLL	Allows for accurate compensation of fly-by timing at start up.

Silicon Results

The Rapid Bridge DDRIII LiquidPHY is a tightly integrated subsystem that minimizes the interaction of many interdependent parameters between different analog, mixed-signal and digital blocks. Additionally, this subsystem may benefit from RBIP0 and RBCPR technologies, which yield an overall power reduction of up to 40% (as shown below).



DDRIII Line Loopback @ 1.4Gbps, silicon results



DDRIII 72-bit PHY Write Leveling

For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at: sales-support@rapidbridge.com or visit www.rapidbridge.com