

## Clock Multiplier PLL A/B/C/D

v1.2

### Features / Benefits

- 100-1800MHz output clock frequency
  - A: 100-400MHz
  - B: 300-700MHz
  - C: 600-1400MHz
  - D: 1000-1800MHz
- 2-bit pre-divider and 5-bit Multiplier
- <10mW power dissipation
- Multiple copies of output clock @1/2, 1/4, and 1/8
- PLL slip function
  - Less than 100µs
- Low Short term jitter
  - $0.01/F_{CLKA}$  ps
- Low Long term jitter
  - $0.05/F_{CLKA}$  ps
- Less than 100ps static phase error from reference clock
- High supply noise rejection
- IDDQ, scan and bypass modes
- Less than ± 2% duty cycle distortion across PVT
- Metal programmable within Rapid Bridge platform
- Spread Spectrum Compliant

### Applications

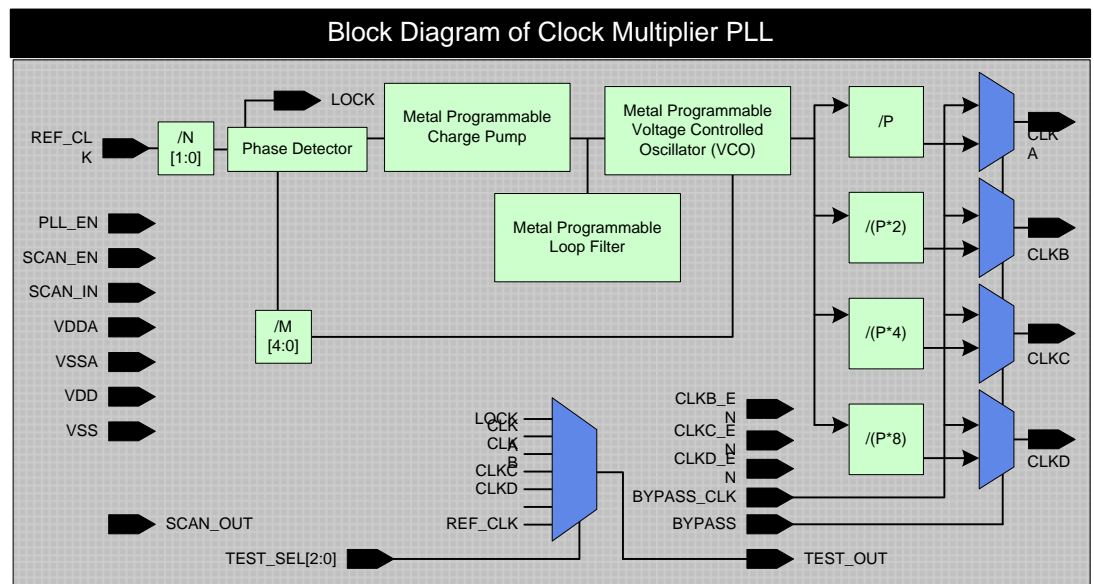
- Frequency synthesis
- Multiple Domain Clock trees
- Cores
  - Logic cores
  - DSPs
  - Processors
- Frequency conversion (Mux/Demux)

### Product Description

Clock Multiplier Phase Lock Loop (CMU PLL) is designed to deliver wide range of internal clock frequencies, 100-1800 MHz, based on a low frequency reference clock, 10-800MHz. The combination of a 2-bit divider, 5-bit multiplier, and 1-bit post divider provides end users fine granularity over the specified frequency range. Multiple copies of the output clock operating at 1/2, 1/4, and 1/8 frequency are phase locked to the main output clock. This addresses applications where multiple clock domains are required. Low static phase error between the multiple output clocks provides an optimum solution for up and down conversion of a data stream. Low short term jitter addresses applications that have tight cycle to cycle timing budgets. Duty cycle correction circuitry enables double edge clocking schemes. Loop bandwidth of the PLL has been set to allow proper multiplication of spread spectrum clocks (SSC). This reduces EMI and substrate noise in many applications.

### An SoC Approach

LiquidMXS is integrated along with LiquidIO and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. Readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs.



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### Complete Timing Block Solution

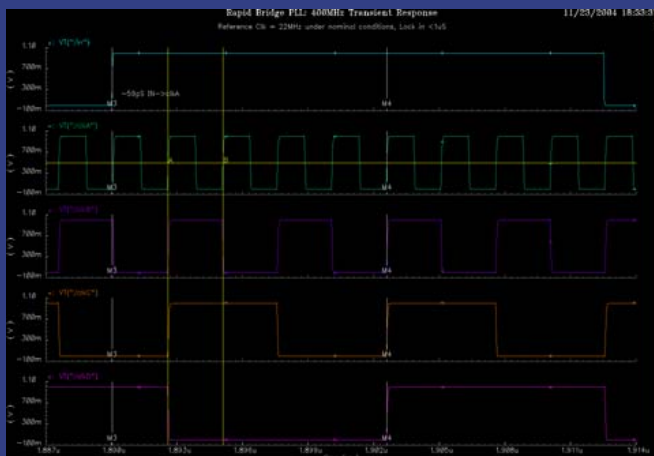
PLL and DLL solutions provide a wide range of performance timing blocks which are tailored for different types of applications. These PLLs and DLLs may serve as frequency synthesizers, de-Skew PLLs, Interface PLLs with multiple phases, and high resolution DLLs for tight timing budgets. Specific jitter parameters are tuned within each family to address specific application requirements.

Clock Multiplier PLLs are implemented with PLL\_EN, BYPASS and SCAN\_EN functions to allow for test and validation of the PLL and the SoC as a complete system. Guidelines have been followed in design and layout to minimize the effect of different sources of noise for optimum performance. Application guidelines are provided within SoC chip and in COT environment to ensure proper integration and performance.

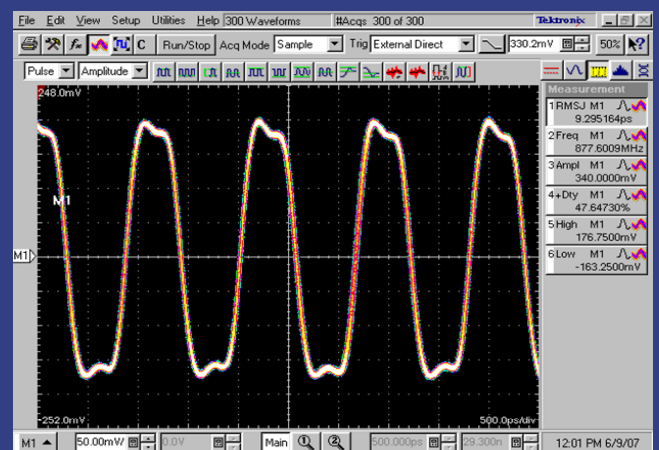
### Performance Beyond the Past

Definition and composition of the different PLL and DLL types is under the umbrella of a complete sub-system definition. The holistic approach in definition, design implementation, physical design and integration result in silicon efficiency that can not be realized through other approaches and results in optimum performance and amortization of analog and Mix-Signal resources available at the chips level. This approach also eliminates so difficult to manage integration issues at the SoC level minimizing potential risks.

Locked CMU PLL A with 22MHz in, 400MHz CLKA to 50MHz CLKD



Silicon results of the Multiplier C PLL @ 880MHz



### For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit [www.rapidbridge.com](http://www.rapidbridge.com)