

Interpolator PLL A/B/C/D

v1.2

Features / Benefits

- 100-1800MHz output clock frequency
 - A: 100-400MHz
 - B: 300-700MHz
 - C: 600-1400MHz
 - D: 1000-1800MHz
- 2-bit pre-divider and 5-bit Multiplier
- <10mW power dissipation
- Multiple copies of output clock @11.25° phase offset
- PLL slip function
 - Less than 100µs
- Low Short term jitter
 - $0.01/F_{CLKA}$ ps
- Low Long term jitter
 - $0.05/F_{CLKA}$ ps
- High supply noise rejection
- IDDQ, scan and bypass modes
- Less than ± 2% duty cycle distortion across PVT
- Metal programmable within Rapid Bridge platform
- Spread Spectrum Compliant

Product Description

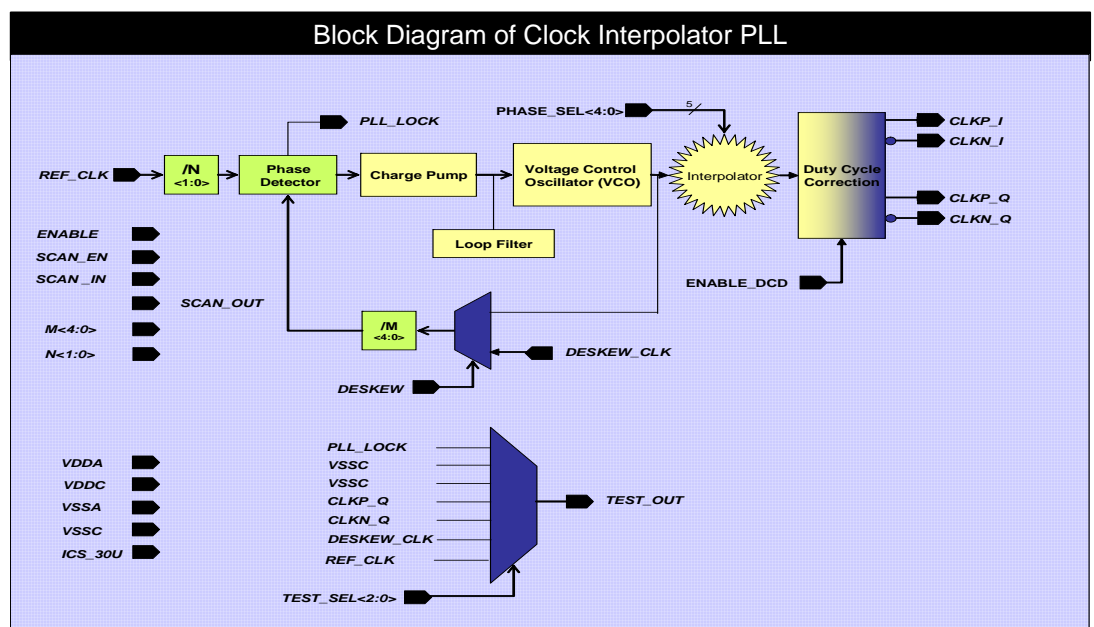
Interpolator PLL family is designed to address accurate edge placement of an outgoing clock signal based on static phase alignment. A phase interpolator is used to provide any one of 32 phase alignments with a resolution of $360^\circ/32$, or 11.25° . The phase alignment may be complemented utilizing external logic algorithms to address clock/data recovery (CDR) or to capture data using training patterns. Different versions of the interpolator PLL (A-E) are provided to address a wide range of operating frequencies, from 200MHz to 1.8GHz, while maintaining adequate phase margins and loop dynamics. Low short and long term jitter improves the overall clock uncertainty and the interface timing budget. Duty cycle correction circuitry enables double edge clocking schemes. The interface PLL family may also be used for internal clock tree de-skewing. Loop bandwidth of the PLL has been set to allow proper multiplication of spread spectrum clocks (SSC). This reduces EMI and substrate noise in many applications.

An SoC Approach

LiquidMXS is integrated along with LiquidIO and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. Readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs.

Applications

- Interface timing
- ppm tracking



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Complete Timing Block Solution

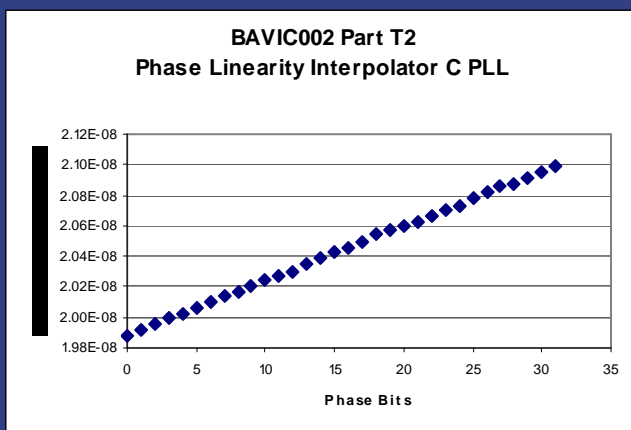
PLL and DLL solutions provide a wide range of performance timing blocks which are tailored for different types of applications. These PLLs and DLLs may serve as frequency synthesizers, de-skew PLLs, Interface PLLs with multiple phases, and high resolution DLLs for tight timing budgets. Specific jitter parameters are tuned within each family to address specific application requirements.

Interpolator PLLs are implemented with PLL_EN, BYPASS and SCAN_EN functions to allow for test and validation of the PLL and the SoC as a complete system. Guidelines have been followed in design and layout to minimize the effect of different sources of noise for optimum performance. Application guidelines are provided within SoC chip and in COT environment to ensure proper integration and performance.

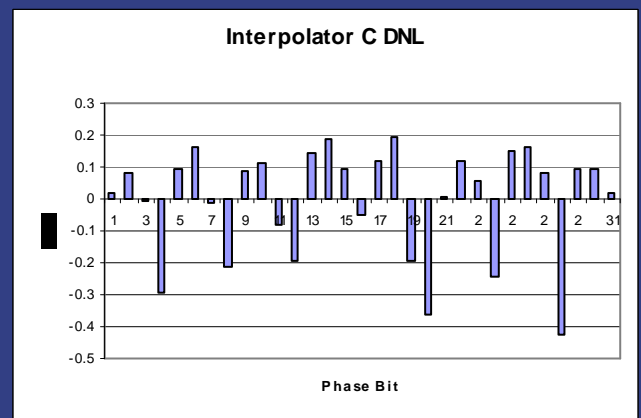
Performance Beyond the Past

Definition and composition of the different PLL and DLL types is under the umbrella of a complete sub-system definition. The holistic approach in definition, design implementation, physical design and integration result in silicon efficiency that can not be realized through other approaches and results in optimum performance and amortization of analog and Mix-Signal resources available at the chips level. This approach also eliminates so difficult to manage integration issues at the SoC level minimizing potential risks.

Silicon results of the phase linearity



Silicon results of the Interpolator PLL C DNL



For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

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