

Triple 10-Bit DAC

v1.2

Features / Benefits

- 14 IO slots for the triple 10-bit configuration
- Up to 500MHz operating
- Full Scale Adjustable
- $\pm 3\text{LSB}$ integral linearity
- $\pm 2\text{LSB}$ differential linearity
- Monotonic
- DAC Enable and Blank functionality
- Optional Pedestal setting
- IDDQ and parametric Nand test functions
- Metal programmable within Rapid Bridge platform
- ESD 2kV HBM, 200V MM, 500V CDM
- Wirebond, Flip Chip and CUP versions available
- IEEE 1149.1 Compliant

Product Description

Triple DAC is a 2.5V supply referenced digital to analog converter, intended to drive 0-19.2mA of current over three channels to 75Ω double terminated lines (37.5 Ω total). The triple-DAC was designed mainly to drive video signals (0-740mV) for Red, Green, and Blue channels, but it may be used in many applications. The DACs can operate up to 500MHz, using 3 10-bit registered inputs, which are latched on the positive edge of an input clock. The output is guaranteed to be monotonic and within $\pm 2\text{LSB}$ over the full operating range.

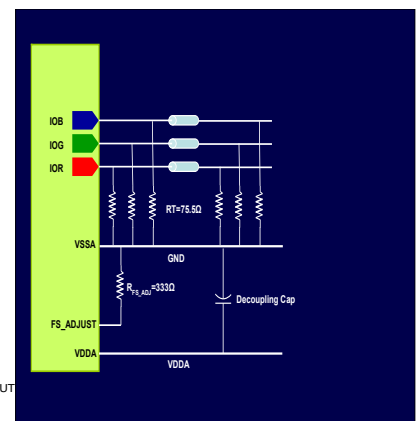
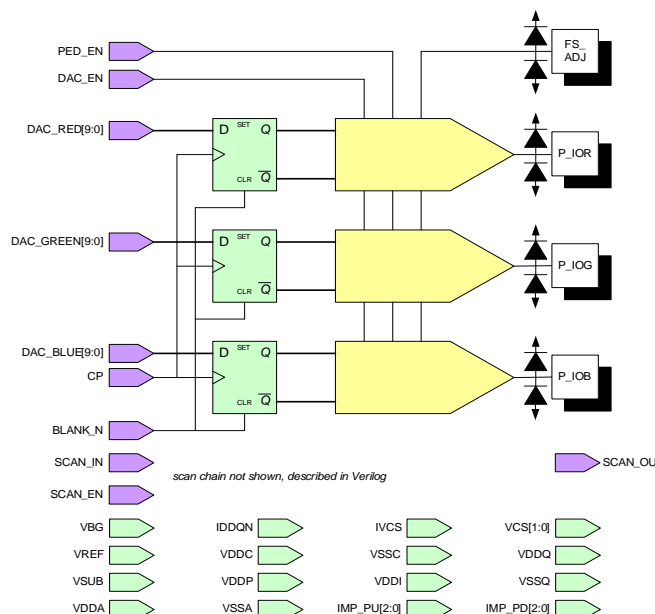
A full-scale adjust pin (FS_ADJ) is provided to set the reference current using an external 333 W resistor, and the internal bandgap on the Rapid Bridge Platform is used to provide a 1.2V reference voltage. If the DAC is used in a COT flow, this voltage must be provided from a source on the chip. This component is used in the IO ring, just like any other output pad, and attaches to readily available power and ground rings on the chip perimeter.

An SoC Approach

LiquidIO is integrated along with LiquidMXS and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. The readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs.

Applications

- Video/Graphics DAC
- General DAC



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Complete Interface Solution

Digital to Analog Converter interfaces is part of a complete IO ring solution, which has been specifically designed for high performance, easy chip integration, and flexible system level requirements. This top-level integrated IO design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection.

Because the IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines.

Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design. IOCalculator software is a WEB based tool that allows end users to calculate power pad requirements based on packaging and system specifications for the supported standard within the Rapid Bridge LiquidIO family. RingComposer is used to compose the entire ring and the respective support circuits based on output of the IOCalculator. Test functions are composed and are correct by construction. The system level ESD results in better than 2kV HBM, 200V MM and 500V CDM models. The combination of the above tool sets and metal programmability creates a complete liquid infrastructure allowing full flexibility and re-programmability.

For More Information . . .

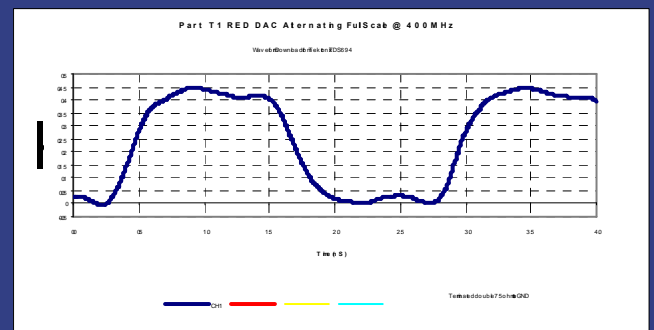
Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com

Performance Beyond the Past

Video DAC is part of a harmonious system that is calibrated through a Central Calibration Unit across process and temperature. This yields significant improvement in rms and peak currents of up to 60%, reducing top level system requirements. Reduction in power is coupled with well matched and balanced output impedances that enhances signaling and performance throughout the system. Systematic implementation of LiquidIO subsystem eliminates potential, difficult to address, interface interactions.

Silicon results of the DAC, full scale toggling @400MHz



Silicon results of the DAC, Differential and Integral Linearity

