

SSTL2 Classi and Classii IO Cell

v1.2

Features / Benefits

- JESD8-9b compliance
- 400MHz/800Mbps data rate
- Independent dynamic pull up and pull down calibration
- IDDQ, parametric Nand and JTAG test functions
- Metal programmable within Rapid Bridge™ platform
- 35µm pad pitch
- ESD 2kV HBM, 200V MM, 500V CDM
- Single ended and differential transceivers with single and differential core signaling
- Less than ±3% duty cycle distortion across PVT
- Wirebond, Flip Chip and CUP versions available
- IEEE 1149.1 Compliant

Applications

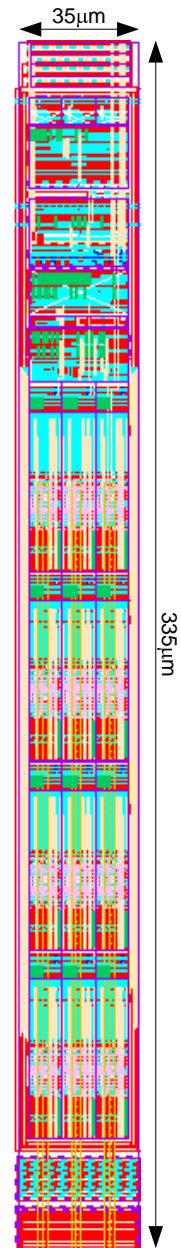
- DDR memory interfaces governed by JESD79C
- DDR memory interfaces for SDRAM, DRAM and FCRAM
- DDR logic interfaces such as XGMII
- General purpose interface

Product Description

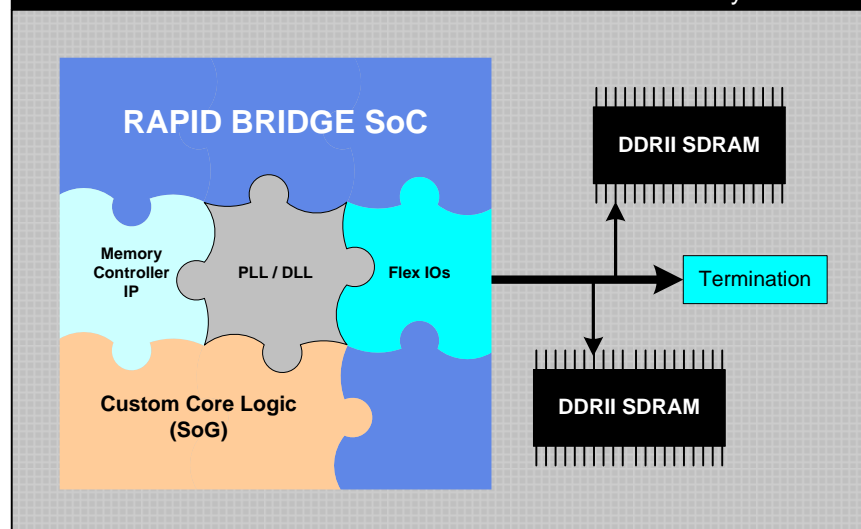
Series Stub Terminated Logic is a 2.5V supply referenced IO interface for digital integrated circuits. It is particularly intended to improve operation in situations where buses must be isolated from relatively large stubs, as defined by JESD8-9. A combination of series and single/parallel termination schemes is used to achieve adequate signaling for different multi-drop bus and point-to-point applications, which addresses different system cost structures and required performance levels.

An SoC Approach

SSTL2 interface has been specifically designed to compliment Rapid Bridge Interface PLLs and DLLs. This enables end users to meet a wide range of memory and logic interfaces up to 800Mbps. Readily integrated system addresses many challenges and concerns associated with high speed interface designs.



SSTL2 Classii double-terminated IO used for DDRII Memory Interface



SSTL2 ClassI and ClassII IO Cell

Complete Interface Solution

SSTL2 interface is part of a complete IO ring solution, which has been specifically designed for high performance, easy chip integration, and flexible system level requirements. This top-level integrated IO design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection.

Because the IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines.

Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design.

Multiple Degrees of Freedom

Unlike FPGA or SA solutions, there are no pre-defined banks for IOs. Designers have the freedom to metal program exactly as many SSTLs and other interface types as are needed for the design, defining the number of power, ground, or support pads for the best system performance. The exact same Interface blocks can be used on both SoC chip, and in a COT environment. This negates any risk in going from sample solution to production.

Soft IP Core Partnership

Partnerships with leading Soft IP vendors provide the end users with an additional layer of risk reduction to address their SoC requirements. Proven memory controllers for different memory configurations and types are available through our soft IP partners.

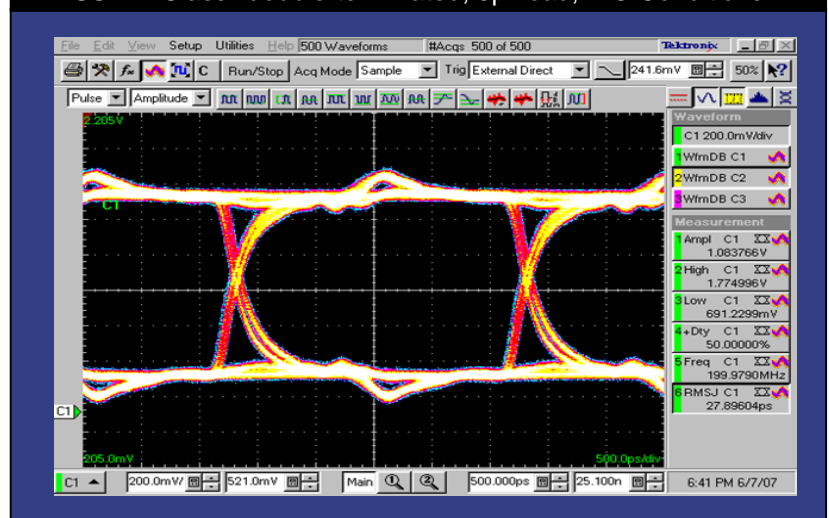
System optimization and performance

Design feature sets allow for system optimization to meet different speed / power products.

Testability feature sets enable the end user with easy and complete validation and production solutions.

IOs have been fully simulated across PVT corners, and silicon proven to be reliable not only as IP, but integrated with other Rapid Bridge and partner products.

SSTL2 ClassII double-terminated, 5pf load, WC Conditions



For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com