

PCI-X Mode1 and 2 IO Cell

v1.2

Features / Benefits

- PCI_X Rev 2.0a
- 266/533MHz mode1/mode2 operations
- Programmable 8.2kΩ pull-up pin for bus keeper applications
- IDDQ, parametric Nand and JTAG test functions
- Multiple logical implementations to simplify system composition.
- Less than ± 3% duty cycle distortion across PVT
- 35μm pad pitch
- ESD 2kV HBM, 200V MM and 500V CDM
- 1.5/3.3V signaling
- Wire-bond, Flip Chip and CUP versions available
- IEEE 1149.1 Compliant

Applications

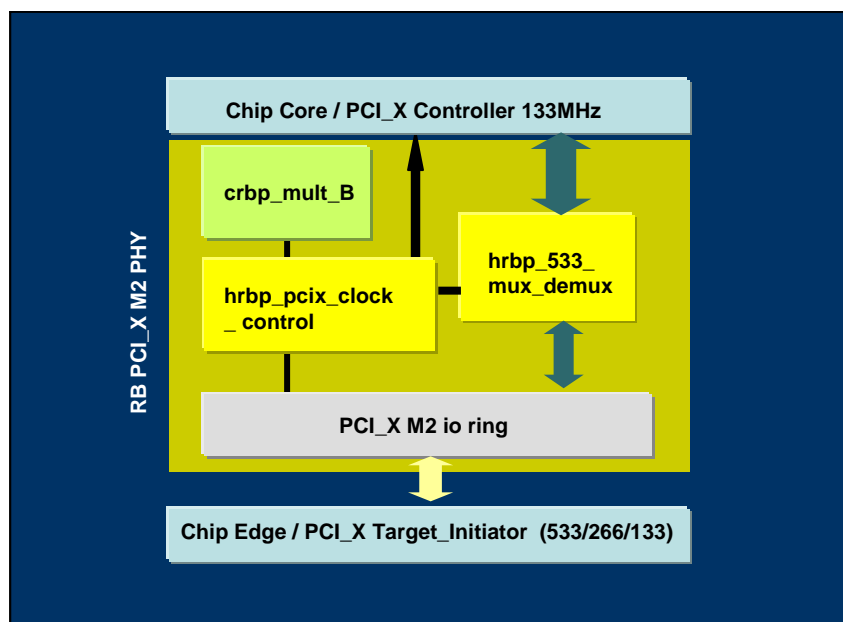
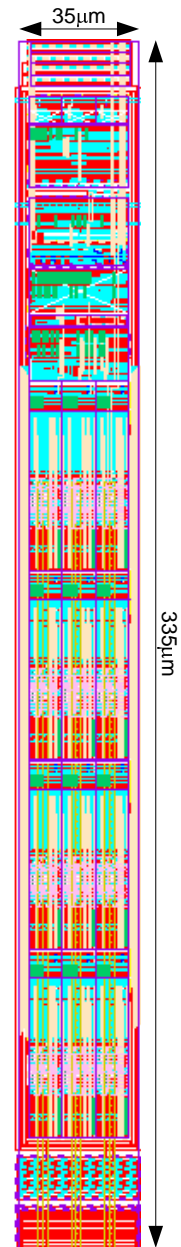
- PCI_X Mode 1 and 2 interface

Product Description

PCI_X Mode 1 and Mode 2 are a 3.3V and 1.5V supply referenced IO interface for digital integrated circuits. PCI_X is an extension to PCI33 and 66 and operated at data rates of 266 and 533 MHz for the Mode 1 and 2, respectively. This design is in accordance with PCI_X Electrical and Mechanical Addendum, Rev 2.0a. PCI-X Mode 1 and 2 are not backward compatible and are not intended for 5V tolerant applications. PCI-X Mode 1 and 2 interface types are used in conjunction with other LiquidIP blocks to compose PCI_X subsystems.

An SoC Approach

LiquidIO is integrated along with LiquidMXS and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. Readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs.



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Complete Interface Solution

PCI_X Mode 1 and interfaces are part of a complete IO ring solution, which has been specifically designed for high performance, easy chip integration, and flexible system level requirements. This top-level integrated IO design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection.

Because the IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines.

Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design. IOCalculator software is a WEB based tool that allows end users to calculate power pad requirements based on packaging and system specifications for the supported standard within LiquidIO family. RingComposer is used to compose the entire ring and the respective support circuits based on output of IOCalculator. Test functions are composed and are correct by construction. System level ESD results in better than 2kV HBM, 200V MM and 500V CDM models. Combination of the above tool sets and metal programmability creates a complete liquid infrastructure allowing full flexibility and re-programmability.

For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com

Performance Beyond the Past

PCI_X is part of a harmonious system that is calibrated through a Central Calibration Unit across process and temperature. This yields significant improvement in rms and peak currents of up to 60%, reducing top level system requirements. Reduction in power is coupled with well matched and balanced output impedances that enhances signaling and performance throughout the system. Systematic implementation of LiquidIO subsystem eliminates potential, difficult to address, interface interactions.

Silicon results for PCI_X Mode1 @ 266MHz

