Product Brief

LiquidIO™

Low Voltage CMOS (LVCMOS) IO Cell

v1.3

Features / Benefits

- EIA/JESD 8-5 normal and wide range compliance
- EIA/JESD 8-7 normal and wide range compliance
- EIA/JESD 8-11 normal and wide range compliance
- Logic programmable drive strength; 2/4/8/12mA
- Up to 150MHz operation
- Independent dynamic pull up and pull down drive strength calibration
- Programmable pull up and pull down structures
- IDDQ, parametric Nand and JTAG test functions
- Metal programmable within Rapid Bridge™ platform
- 35µm pad pitch
- ESD 2kV HBM, 200V MM and 500V CDM
- Wirebond, Flip Chip or CUP versions available
- IEEE 1149.1 Compliant

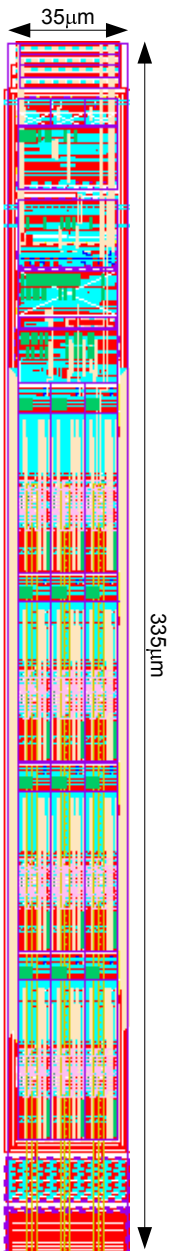
Applications

- General purpose interface
- Mobile SDRAM interface
- CellularRAM Memory interface

Product Description

The Rapid Bridge Low Voltage CMOS is 1.08v to 2.7v supply referenced, un-terminated IO buffer interface targeted for low performance, low cost, general purpose applications. This pad set provides metal-programmable drive strengths from 1 to 16mA to meet different application requirements beyond those specified by EIA/JESD8-5 and 8-7. Different output impedance settings are available for a wide range of drive applications, from 35 to 60Ω (controlled through on-die calibration); this includes a core-programmable 24kΩ pull-up or pull-down pin for applications that require a high-impedance rail termination (thus eliminating the need for external components).

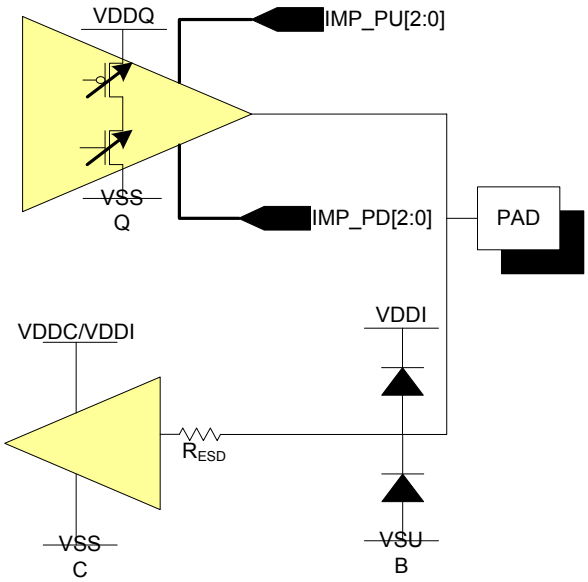
The receiver's hysteresis can be enabled/ disabled through a core-programmable pin. The LVCMOS IOs are fully bi-directional, with optional OE and IE to make input or output-only versions. The LVCMOS interface supports a wide range of VDDQ levels (from 0.9V to 2.7V). The LVCMOS IOs are intended to perform up to 150MHz, using VDDQ supply voltages down to 1.4V or 75MHz when the VDDQ supply voltage is allowed down to 1.08V.



An SoC Approach

LiquidIO is ideally integrated with LiquidMXS and LiquidCell subsystems to create highly integrated, efficient and comprehensive LiquidPHY subsystems. These readily integrated subsystems address the greatest associated with high-speed interface designs.

LVCMOS Block Diagram



Product Brief

LiquidIO™

Low Voltage CMOS (LVCMOS) IO Cell

Complete Interface Solution

The LVCMOS interface is part of a complete IO ring solution that has been specifically designed for high performance, easy chip integration, and flexible system-level requirements. This integrated SoC design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection. System-level ESD results in better than 2kV HBM, 200V MM and 500V CDM models.

Because the IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines.

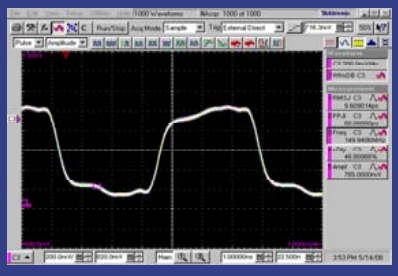
Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design. This software allows end users to calculate power pad requirements based on packaging and system specifications for the supported standard within the Rapid Bridge LiquidIO family. It can also be used to compose the entire ring and the respective support circuits based on power requirements. Test functions are composed and are correct by construction.

The combination of the above tools and metal programmability creates a complete “liquid” infrastructure that allows full flexibility and re-programmability.

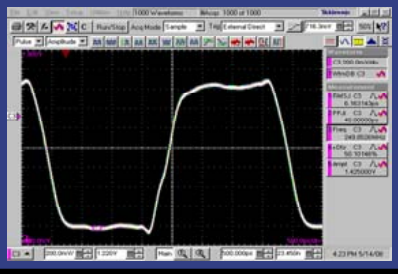
Performance Beyond the Past

LVCMOS is part of a harmonious SoC system that is calibrated through a Central Calibration Unit across process and temperature. This yields significant improvement in rms and peak currents of up to 60%, reducing top-level system requirements. This reduction in power is coupled with well-matched and balanced output impedances that enhance signaling and performance throughout the system. A systematic implementation of LiquidIO subsystems addresses the greatest challenges of design for interface interactions.

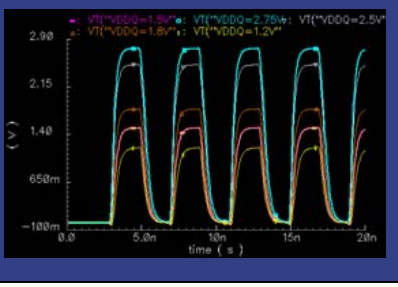
LVCMOS, 1.2V, 50Ω termination to GND



LVCMOS, 1.8V, 50Ω termination to GND



LVCMOS, unterminated, 10pf load



For More Information. . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com