

HSTL Classi and Classii IO Cell

v1.2

Features / Benefits

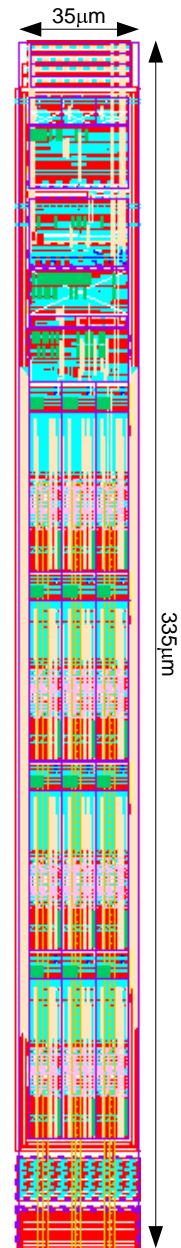
- JESD8-6 compliance
- Up to 500MHz/1Gbps data rate
- Independent dynamic pull up and pull down calibration
- Half and full strength driver option
- IDDO, parametric Nand and JTAG test functions
- Multiple logical implementations to simplify system composition.
- Less than $\pm 3\%$ duty cycle distortion across PVT
- 35 μ m pad pitch
- ESD 2kV HBM, 200V MM and 500V CDM
- 1.5/1.8V signaling
- Wire-bond, Flip Chip and CUP versions available
- IEEE 1149.1 Compliant

Product Description

High Speed Transceiver Logic is a 1.5V/1.8V supply referenced IO interface for digital integrated circuits. HSTL standard IO places high priority on flexibility and technology independence allowing for a broad range of applications. Speed of operation and flexibility of the supply and reference voltages along with differential and single ended options allow this interface to be used in conjunction with different interface types (such as SSTL18 or PECL). Single/parallel termination schemes are used to achieve adequate signaling for different multi-drop bus and point-to-point applications, and to allow tradeoffs between system costs and required performance levels.

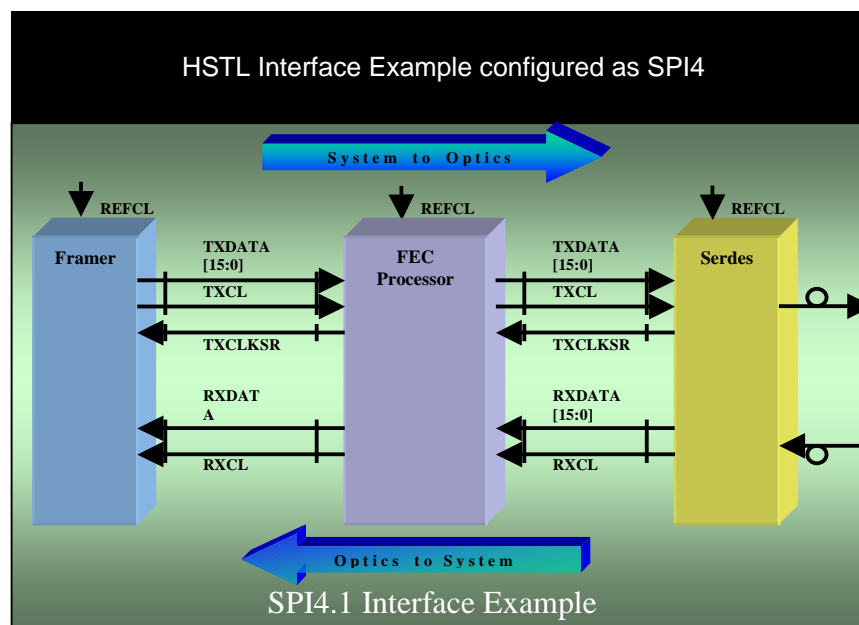
An SoC Approach

LiquidIO is integrated along with LiquidMXS and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. Readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs.



Applications

- RDRAM, QDR SRAM, DDR/SDR SRAM
- Mobile SDRAM
- SPI4 Phase I, XGMII
- High speed interfaces up to 600MHz
- Backplane, Box to Box communication
- 10GbE, FC, XENPAK, XPAK



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Complete Interface Solution

HSTL interface is part of a complete IO ring solution, which has been specifically designed for high performance, easy chip integration, and flexible system level requirements. This top-level integrated IO design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection. Because the IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines. Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design. IOCalculator software is a WEB based tool that allows end users to calculate power pad requirements based on packaging and system specifications for the supported standard within the Rapid Bridge LiquidIO family. RingComposer is used to compose the entire ring and the respective support circuits based on output of the IOCalculator. Test functions are composed and are correct by construction. System level ESD results in better than 2kV HBM, 200V MM and 500V CDM models. Combination of the above tool sets and metal programmability creates a complete liquid infrastructure allowing full flexibility and re-programmability.

For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com

Performance Beyond the Past

HSTL is part of a harmonious system that is calibrated through a Central Calibration Unit across process and temperature. This yields significant improvement in rms and peak currents of up to 60%, reducing top level system requirements. Reduction in power is coupled with well matched and balanced output impedances that enhances signaling and performance throughout the system. Systematic implementation of LiquidIO subsystem eliminates potential, difficult to address, interface interactions.

