

DDRIII IO Cell

v1.2

Features / Benefits

- JESD79-3A compliance
- On Die Termination (ODT)
- Off Chip Driver(OCD) Impedance Adjust
- 1.066/1.333Gbps data rate
- Independent dynamic pull up and pull down calibration
- 34/40Ω driver option
- IDDQ, parametric Nand and JTAG test functions
- Multiple logical implementations to simplify system composition.
- Less than ± 3% duty cycle distortion across PVT
- 35μm pad pitch
- ESD 2kV HBM, 200V MM and 500V CDM
- Wire-bond, Flip Chip and CUP versions available
- IEEE 1149.1 Compliant

Applications

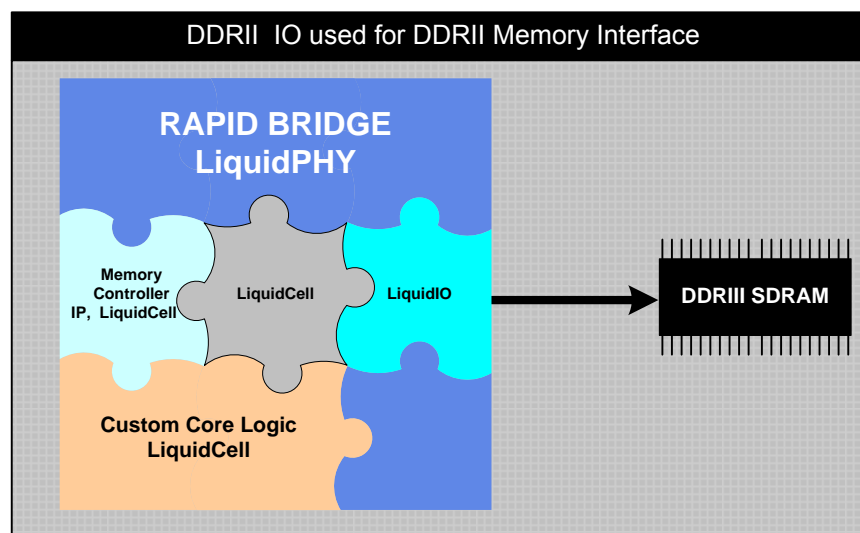
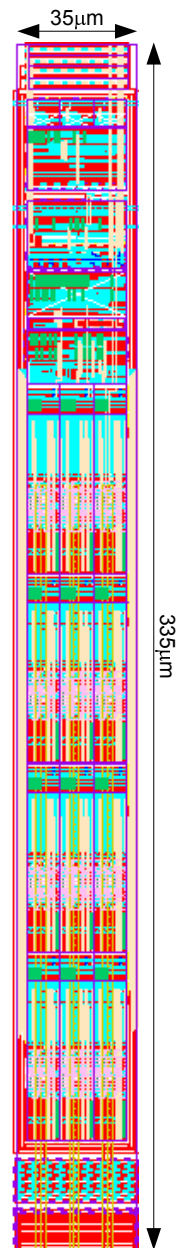
- DDRIII memory interfaces governed by JESD79-3A
- DDRIII memory interfaces for SDRAM, DRAMIII and RLDRAMIII -- 400/533/667/800/1066Mbps
- High Speed Interfaces up to 800MHz
- PC Graphics, Consumer

Product Description

DDRIII, Series Stub Terminated Logic, is a 1.5V supply referenced IO buffer interface for digital integrated circuits. It is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. DDRIII IO pad set is designed in accordance to JESD79-3A in order to enable high-speed memory operation by providing On Die Termination (ODT) that may be set to different values. ODT feature is designed to improve signal integrity in the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. A default calibrated driver in the full-strength mode results in an output impedance value of 40Ω or 34Ω. DDRIII is intended to be technology independent for different multi-drop bus and point-to-point applications. DDRIII IO set is designed for a 1.5V signal level with calibrated 34/40Ω output impedance. High operating frequencies are achieved through independent on-die calibration of the output impedance for the rise and fall transitions to maintain adequate duty cycle. Calibrated on die parallel 120Ω, 60Ω, 40Ω, 30Ω and 20Ω far-end terminations eliminate the need for external components while improving system noise margins by providing termination as close to the die as possible.

An SoC Approach

LiquidIO is integrated along with LiquidMXS and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. Readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs.



DDRIII IO Cell

Complete Interface Solution

DDRIII interface is part of a complete IO ring solution, which has been specifically designed for high performance, easy chip integration, and flexible system level requirements. This top-level integrated IO design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection.

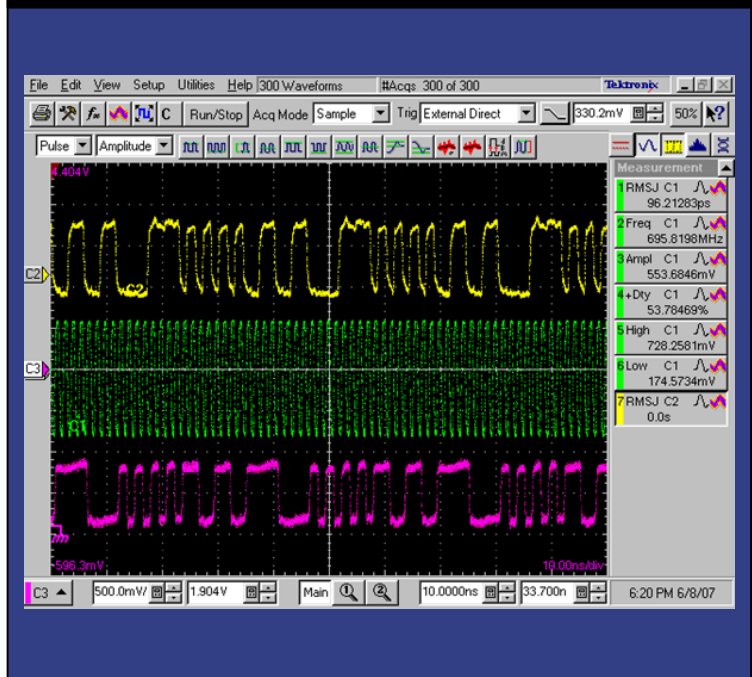
Because the IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines.

Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design. IOCalculator software is a WEB based tool that allows end users to calculate power pad requirements based on packaging and system specifications for the supported standard within the Rapid Bridge LiquidIO family. RingComposer is used to compose the entire ring and the respective support circuits based on output of the IOCalculator. Test functions are composed and are correct by construction. System level ESD results in better than 2kV HBM, 200V MM and 500V CDM models. Combination of the above tool sets and metal programmability creates a complete liquid infrastructure allowing full flexibility and re-programmability.

Performance Beyond the Past

DDRIII is part of a harmonious system that is calibrated through a Central Calibration Unit across process and temperature. This yields significant improvement in rms and peak currents of up to 60%, reducing top level system requirements. Reduction in power is coupled with well matched and balanced output impedances that enhances signaling and performance throughout the system. Systematic implementation of LiquidIO subsystem eliminates potential, difficult to address, interface interactions.

Silicon results of DDRIII, 1.4Gbps input / output pattern and clock, 50Ω termination to ground



For More Information . . .

Regarding LiquidIP[™], LiquidASIC[™], or LiquidSoC[™], please contact Rapid Bridge at:

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