

LiquidCell SoG Library

v1.5

Features / Benefits

- Customized transistor sizes for each process
- Synthesize logic up to 800MHz
- Area efficient library of over 700 elements with 160+ functions
- Ready for DFT / ATPG with scan technology
- Low power 1.0V or 1.2V VDDC, from -40 to 125C
- Gates not used for logic are made into decoupling capacitors or fillers
- Uses conventional COT flow for synthesis, P&R, modeling, etc.
- Full clock tree insertion support
- Allows radical reduction in cycle time by using only metal to configure
- Allows major logic changes by updating only metal mask
- Very low risk. Low cost, high yield design solution
- Full modeling support provided
- Support for 2-pass multi-Vt

Applications

- Any synthesizable core logic up to 800MHz
- Rapid Bridge™ LiquidSoC, LiquidASIC, or standard COT ASIC flow
- Custom placement for faster speed

Product Description

LiquidCell consists of a metal-programmable sea of gates (SoG) that can be configured into millions of usable elements from a library of over 700 standard cells. The cell list comprises of the most commonly used elements in standard synthesis libraries from leading IP vendors. Translation tables and tools are provided for mapping into the standard common libraries providing competitive performance and seamless transition to customer's internal flows.

The LiquidCell library can be run through any standard synthesis and Place & Route (P&R) flow, or synthesized cores can be converted to LiquidCell cores by using the provided translation tables.

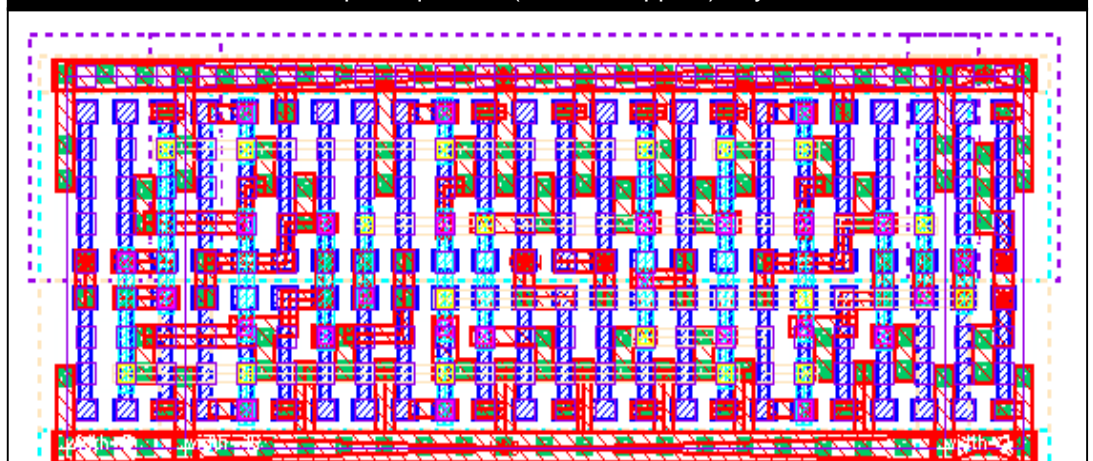
LiquidCell may be used for any ASIC design without any restrictions.

An SoC Approach

LiquidCell library has been designed to work within SoC environment including RapidBridge Liquid platforms, which (with its readily integrated system) addresses many challenges and concerns associated with high- speed designs. Signal integrity software can be used on custom blocks to attain even higher speeds. The LiquidCell core is fast enough to synthesize register maps and any other block that might otherwise require custom circuitry.

The LiquidCell library is fully ATPG / DFT- compliant and supports clock tree insertion. The entire system is designed to work together.

Sample LiquidCell (srbs_sfcnqqnd2) Layout





LiquidCell SoG Library

Complete SoC Solution

LiquidCell library has been designed to offer superior performance without compromising area or power. Larger balanced cells are provided for special data paths.

The Sea of Gates solution allows users to make full logic changes by just using metal masks, saving time and cost normally associated with chip spins.

LiquidCell is available at TSMC 90 nm, 65 nm and 45/40 nm.

Multiple Degrees of Freedom

Unlike FPGA or SA solutions, there are no pre-defined logic blocks or macrocells. Designers have the freedom to make blocks exactly the size they need, eliminating extra pipes, power, and inefficiency associated with macrocell design.

Also, the exact same blocks can be used both on LiquidASIC, LiquidSoC, or in a COT environment. This negates any risk in going from sample solution to production.

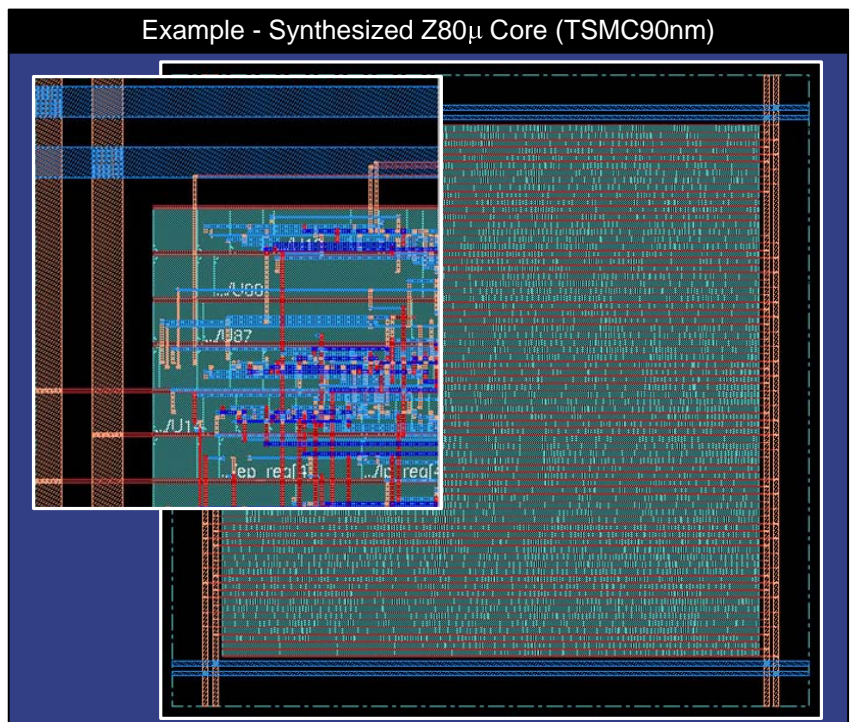
Designers also have the freedom to use specialized processes, such as low power, high speed, or set V_T to meet special application needs.

Soft IP Core Partnership

Partnerships with leading Soft IP vendors provide end users with an additional layer of risk reduction to address their SoC requirements. Pre-synthesized or RTL cores can be imported directly into the library and placed on the SoC.

System Optimization and Performance

LiquidCell platform is designed to provide much higher performance than commonly used programmable gate arrays and single metal structural arrays. Fabrication time, flexibility, and cost are vastly improved from COT and ASCII flows. For a specific list of cells, functions, and drive strengths, see the Rapid Bridge LiquidCell documentation.



For More Information. . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com