

## RB1010 & RB1020S Families

v1.3

### Benefits

- Very Low NRE
- Lower Risk
- Flexible & Scalable Resources
- Vast Proven IP selection
- Large Selection of Preset Slices
- Turnkey (RTL handoff)
- Fast Turn around Time  
Typically 16 Weeks from RTL
- Scalable Volume - Low (1000)  
- High Volume (1-5M)
- Metal programmable
- Standard & Custom Package Options
- Embedded Soft CPU ARM926 EJS

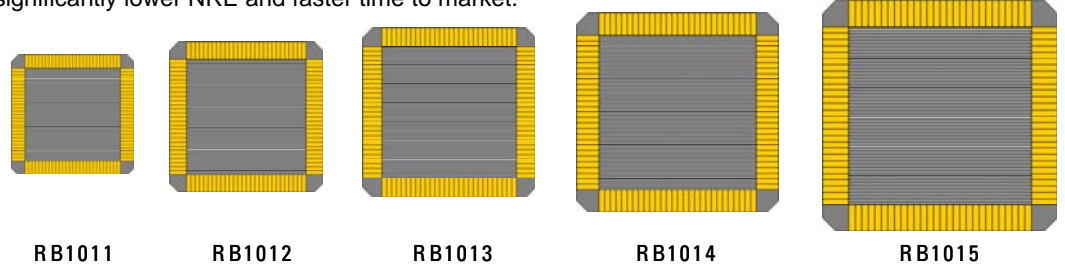
### Product Description

LiquidASIC is the industry's highest performing flexible family of ASIC platforms enabling a new paradigm of true ASIC/COT performance, flexibility and least time to market.

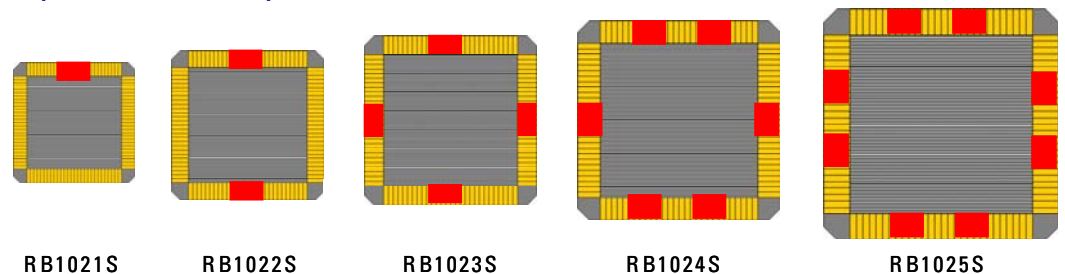
LiquidASIC is an advanced ASIC platform utilizing a combination of metal programmable LiquidIP, our patented Core Power Reduction (RBCPR™) Low Power option and Industry Standard EDA tools to deliver a high performing ASIC design while reducing cost, time to market and risk.

At the heart of our innovative LiquidASIC technology is the highly customizable LiquidIP { IOs, Complex PHYs, Mixed Signal, Sea of Transistors Logic section, SerDes and Memories }. Unlike traditional Structured ASICs or FPGAs, our integrated solution gives our customers complete freedom to tailor their designs much like any Standard Cell approach. LiquidASIC enables COT type capability and flexibility previously only available to Custom SoCs.

LiquidASIC is identical to custom SoCs in Density, Power and Performance but benefits from significantly lower NRE and faster time to market.

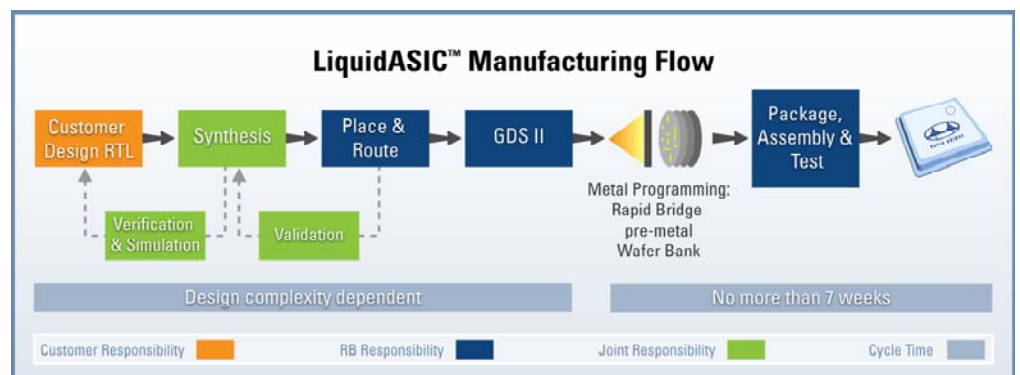


### LiquidASIC family with & without SerDes



### Applications

- Consumer
- Telecom
- Storage
- Mobile
- Computing
- Medical
- General Purpose





## RB1010 & RB1020S Families

### Features

#### LiquidIO

- LVCMOS/LVTTL
- SSTL15/18/SSTL2
- HSTL I/II
- LVDS
- TMDS
- CML
- PCIx
- PECL
- RLDRAM I/II & QDR2

#### LiquidPHYs

- DDR2/DDR3
  - Many Configurations
- RLDRAM I/II
- MDDR
- QDR
- SDRAM
- USB2.0 OTG
- HDMI
- PCIx
- Ethernet Interfaces
- RGMII
- SGMII

#### LiquidSerDes

- PCIe (Gen1& 2)
- SATA (1 & 2)
- XAUI
- Serial Rapid IO L½
- FiberChannel
- Infiniband

#### LiquidMXS

- 15 types of PLLs (20MHz. - 2GHz.)
- VDAC 10-bit
- Large # of DLL types
- Band Gap

#### LiquidCell

- Sea of Transistors
- >700 standard library elements
- 700Mhz (24 levels of logic)

#### LiquidMemory

- Register Files up to 8Kbits – single/multi port configs.
- High Density compiled Metalized SRAM

### Complete SoC Solution

LiquidASIC portfolio of pre-configured master slices offers the industry's most flexible programmable IP and resources. With our tightly integrated IP solutions, LiquidASIC simplifies ASIC/ASSP design efforts for all market segments. LiquidASIC family of products is offered with SerDes and without SerDes in addition to Rapid Bridge Core Power Reduction™ (RBCPR) Technologies

LiquidASIC	RB1011	RB1012	RB1013	RB1014	RB1015
Total IOs	530	724	1040	1244	2060
Gate Count (Mgates)	5.6	11.2	22.4	33.6	50.4
Memory (Mbits)	5.79	11.58	23.16	34.75	52.12
1Kx36	86	172	344	516	774
8Kx32	10	20	40	60	90
1RW/1R1W Register File (Gates/Bit)	3.5	3.5	3.5	3.5	3.5
One Time Programmable (Kbits)	8	16	32	48	72
1Kx8	1	2	4	6	9
Analog Sites	7	14	28	42	63
ARM926EJ_S	√	√	√	√	√

LiquidASIC	RB1021S	RB1022S	RB1023S	RB1024S	RB1025S
Total IOs	468	600	792	872	1786
Gate Count (Mgates)	5	10	20	30	45
Memory (Mbits)	5.27	10.55	21.10	31.65	47.48
1Kx36	72	144	274	432	648
8Kx32	14	28	56	84	126
1RW/1R1W Register File (Gates/Bit)	3.5	3.5	3.5	3.5	3.5
One Time Programmable (Kbits)	8	16	32	48	72
1Kx8	1	2	4	6	9
Analog Sites	7	14	28	42	63
Serdes Lanes	4	8	16	24	36
ARM926EJ_S	√	√	√	√	√

### Packaging Information

Our standard packaging are 208 pin TFBGA, 324 pin FP BGA, 456 pin PBGA, 676 pin FP BGA, 1153 pin FP BGA, 1760 pin FP BGA. Additionally Custom packaging is available on request.

For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact

Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com